24 July 2019

EEL 3712L LOGIC DESIGN I LAB

Final Exam – Summer, 2019 Instructor: Abdullah Aydeger

Student Name: PID:

In order to get (partial) credit, please do not leave any step/question empty. Please use **minimized** schematic in your designs for full credits.

For the programming questions: if your board does not work, send all source code in .tex format to aaydeger@fiu.edu to get partial credits. (Do not expect to earn more than half points available). You are also welcome to run your program as a simulation instead of board implementation if you want to.

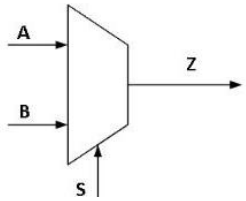
Question 1: (45 points)

(a) What is full-adder? Explain in short by showing its truth table. (5 points)

(b) Write the equation for full-adder outputs in terms of inputs and draw the schematic. (5 points)

(c) What is multiplexer? Explain in short by showing the truth table of 4 to 1 MUX. (5 points)

(d) Draw the 4 to 1 MUX as a following box, showing all inputs and outputs. (5 points)



(e) Design and draw one-bit full-adder by using 4 to 1 MUX(es) and any logic gate(s). (10 points)

(f) Implement the schematic on board. **Make sure** to show your board implementation working in the class to get a grade for this option. If you could not make the design in step 'e', make full-adder by using schematic in 'b' step. Remember you will lose 5 points if you implement 'b' instead of 'e'. (15 points)

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Question 2: (40 points)

(a) What is the decoder? Explain in short by showing the truth table of 3 to 8 decoder. (5 points)

(b) Draw the 3 to 8 decoder showing all inputs and outputs. (5 points)

(c) Write the equation for each output (D0, D1, … D7) of the 3 to 8 decoder in terms of inputs. (5 points)

(d) Please implement and draw the following function using 3 to 8 decoder: f(a,b,c) = (a'+b)(b'+c)(a+c) (10 points)

(e) Implement the schematic in 'd' on board. **Make sure** to show your board implementation working in the class to get a grade for this option. If you could not make the design in step 'd', you can implement 'c' step (a regular 3 to 8 decoder). Remember you will lose 5 points if you implement 'c' instead of 'd'. (15 points) (15 points)

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Question 3: (15 + 30 points)

(a) Write the equation for the output of the 4 to 1 MUX in terms of inputs. (5 points)

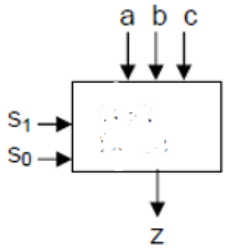
(b) Write the equation for the output of the 8 to 1 MUX in terms of inputs. (5 points)

(c) Draw the full schematic of 4*1 MUX by using AND, OR, INVERTER gates (whichever needed). (5 points)

Extra Part:

(d) Design and draw 8 to 1 MUX using 4 to 1 MUX(es) and/or 2 to 1 MUX(es). (5 points)

(e) Implement the following function with any size MUX(es) and any logic gates you need. 3 data inputs as (a, b, c) and 2 control inputs as (s0, s1). (10 points)



S_1 S_0	z
0 0	a·c
0 1	b·c
1 0	a+c
1 1	b+c

Hint: (1) Take a look at the equation that you write down for step 'a'. (2) s1 and s0 can be used in different MUXes.

(f) Implement the schematic on board. **Make sure** to show your board implementation working in the class to get a grade for this option. If you cannot design the function in 'e', you can implement 'b' step (i.e., 8 to 1 MUX), remember you will lose 5 points in this case. (15 points)

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Extra Question 4: (20 points)

(a) What is NAND gate? Explain in short by giving 4-input NAND gate truth table. (5 points)

(b) How can we implement 4-input NAND gate using ONLY 2-input NAND gates. (5 points)

(c) Design full adder by using only one decoder of a proper size, and 2-input **NAND** gates. (10 points)